Digital Current Sensorless Control for Dual-Boost Half-Bridge PFC Converter with Natural Capacitor Voltage Balancing

Hung-Chi Chen, *Senior Member, IEEE,* Che-Yu Lu, *Student Member, IEEE,* Guan-Ting Li and Wei-Cheng Chen

***Abstract* — To improve the efficiency of the conventional boost-type power factor correction (PFC) converters with the diode bridge circuit, the PFC converters of bridgeless category are often used. Due to no series-connected switches and no short-through risks, the dual-boost half-bridge (DBHB) circuit is used as the PFC converter in this paper. In order to simplify the conventional two-loop control scheme and reduce the number of sensors, the behaviors of DBHB PFC converter are studied and its equivalent single-switch model is developed. Then, the current sensorless control for DBHB PFC converter is proposed to achieve voltage regulation and yield sinusoidal input current in phase with the input voltage without sensing any current. In addition, the proposed method is able to balance capacitor voltages naturally without adding any voltage balancing control loop. An 800W DBHB PFC prototype is implemented to evaluate the control performance. Both simulation and experimental results are provided to demonstrate the proposed current sensorless control method.**

***Index Terms*— Current Sensorless Control, Dual-Boost Half-Bridge Converter, Power Factor Correction (PFC).**

I. INTRODUCTION

In order to reduce the power transmission loss and improve the power quality, more and more electronic products are required to include the power factor correction (PFC) function. The conventional PFC function is often implemented in the circuit topology - a diode bridge rectifier with a single-switch boost converter in Fig. 1(a) [1-4]. This topology is simple, but it suffers from larger conduction voltage drop and switch power loss than other topologies, such as half-bridge PFC converter [5-6], full-bridge converter [7], and the bridgeless PFC converters in Fig. 1(b) and Fig. 1(c) [8-10].

Recently, the cascade dual-boost converter in [11] had been widely used in some applications, such as the solar power conditioning systems [12] and the intelligent universal transformer [13] due to their high reliability and efficiency [14-15]. From Fig. 1(d), each switch is connected with a diode which enables the cascade dual-boost converter to avoid the short-through problem without including dead-time settings. Moreover, no reverse recovery current flows through the body diode of each switch due to two diodes in the current flowing path. Therefore, the loss of reverse recovery current is obviously reduced. The distinguished features contribute to the advantages of the high reliability and high efficiency for cascade dual-boost converter.

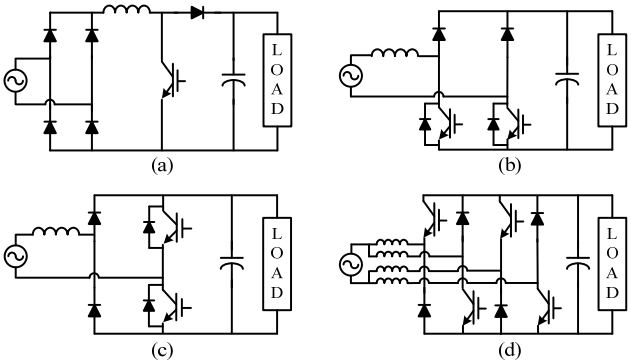

Fig. 1. Boost-type converters: (a) conventional single-switch PFC converter [1-4]; (b) bridgeless PFC converter [8-9]; (c) bridgeless PFC converter [10]; (d) cascade dual-boost AC/DC converter [11-12].

At the same time, the dual-boost half-bridge (DBHB) converter plotted in Fig. 2 can be found in [13-16]. Obviously, DBHB converter has less switches and power loss than the cascade dual-boost converter as shown in Fig. 1(d).

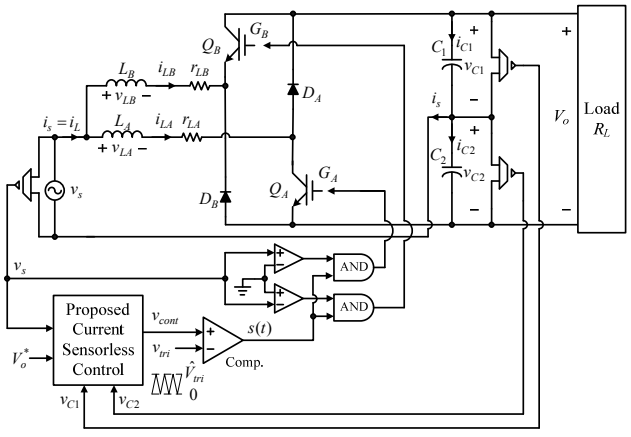

Fig. 2. Dual-boost half-bridge (DBHB) PFC converter with the proposed current sensorless control.

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For PFC application, the conventional two-loop control with the inner current loop and the outer voltage loop can be used to control all the converters in Fig. 1 where it needs to sense the DC-link voltage, the AC voltage and the inductor current. It is noted that the two-loop control can also be used in the half-bridge converters, but it needs to include third control loop to balance both capacitor voltages [6, 17-19]. Therefore, total four sensors (three voltage sensors and one current sensor) are needed to implement the half-bridge PFC converter.

In digital PFC control, the current is conventionally feedback by the current sensor and Analog-to-Digital converter (ADC) with high resolution and high bandwidth. To reduce the cost, some control methods had been proposed in [20-27].

In [20-21], the current sensing methods using only comparators without real A/D converter were proposed. Furthermore, the control methods proposed in [22-23] rebuilt the current feedback signal from the sensed voltages. An adaptive inductor model [24] and the adaptive nonlinear current observer [25] were developed to estimate the current, individually. All the above methods can be classified into two-loop current sensorless control methods.

The methods in [7, 26-29] can be seen as the single-loop current sensorless control methods where only voltage feedback loop is included and the switch duty ratio is synthesized from the controller output and the circuit parameters.

From literatures, no control method had been developed for half-bridge converter due to the requirement of voltage balancing loop. In this paper, the DBHB behaviors have been studied and its single-switch model is developed. Then, the first current sensorless control method for DBHB PFC converter has been proposed. Without including any voltage balancing loop, both capacitor voltages can be balanced naturally by the proposed method. Finally, an 800W DBHB PFC prototype is implemented to evaluate the performances, and some simulation and experimental results are given to demonstrate the performances.

II. Modeling of Dual-Boost Half-Bridge Converter

A. Operation Principle

From Fig. 2, the switch Q_A always turns off when the input voltage is in negative half-cycle $v_s < 0$. The switch Q_B always turns off in the positive half-cycle $v_s > 0$. All the switching states are tabulated in Table I where the corresponding circuits are plotted in Fig. 3.

TABLE I. Summary of Switching States

Input Voltage	States	$s(t)$	Bridge A		Bridge B		C_1	C_2
			G_A	D_A	G_B	D_B		
$v_s > 0$	State 1	High	ON	OFF	OFF		$i_{C1} < 0$	$i_{C2} < 0$
	State 2	Low	OFF	ON			$i_{C1} > 0$	
$v_s < 0$	State 3	High	OFF		ON	OFF	$i_{C1} < 0$	$i_{C2} < 0$
	State 4	Low			OFF	ON		$i_{C2} > 0$

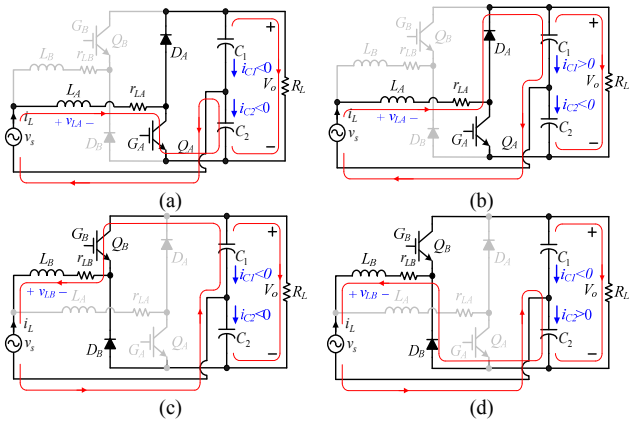

Fig. 3. Switching states of dual-boost half-bridge PFC converter: (a) state 1; (b) state 2; (c) state 3; (d) state 4.

According to the control block diagram as shown in Fig. 2, the switching signal $s(t)$ is generated from the comparison between the control signal v_{cont} and the triangle signal v_{tri}. Thus, the resulting switching signal $s(t)$ can be expressed as in (1). In addition, both gate signals G_A and G_B are synthesized from the switching signal $s(t)$ with the input voltage v_s.

$$s(t) = \begin{cases} 1 & , v_{cont} \geq v_{tri} \\ 0 & , v_{cont} < v_{tri} \end{cases} \quad (1)$$

When the input voltage is positive $v_s > 0$, the gate signal G_A is equal to the switching signal $G_A = s(t)$ and the other gate signal G_B is off. From Fig. 3(a), both capacitor currents are negative $i_{C1} < 0$ and $i_{C2} < 0$ (i.e. both capacitors C_1 and C_2 discharge) in state 1.

In Fig. 3(b), the switch Q_A turns off but the inductor current flows through the diode D_A, and the capacitor current i_{C1} turns to be positive. That is, the capacitor C_1 becomes charged $i_{C1} > 0$, and the other capacitor C_2 keeps discharged $i_{C2} < 0$ in state 2.

In the negative half-cycle $v_s < 0$, the gate signal G_B is equal to the switching signal $G_A = s(t)$ and the other gate signal G_A is off. In state 3, both capacitor currents are negative $i_{C1} < 0$ and $i_{C2} < 0$, and both capacitors C_1 and C_2 discharge as drawn in Fig. 3(c).

Fig. 3(d) shows that the switch Q_B turns off but the inductor current flows through the diode D_B. It follows that the capacitor current i_{C1} remains negative but the current i_{C2} becomes positive in state 4.

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B. Equivalent Single-Switch Model

In order to study the behaviors of the DBHB PFC converter, some assumptions are made as follows:

1) Both inductances and inductor resistances are the same i.e., $L_A = L_B = L$ and $r_{LA} = r_{LB} = r_L$, respectively. Both capacitances are equal $C_1 = C_2 = C$.
2) Both conduction voltage of switches Q_A and Q_B are equal to V_{ON}. In addition, both conduction voltage of diodes D_A and D_B are also equal to V_{ON}.
3) The steady-state output voltage V_o is well regulated to the voltage command V_o^*.
4) Because the switching frequency f_s is much higher than the line frequency f, the input voltage within the switching period $T_s = 1/f_s$ is regarded as the constant value.
5) The converter operates in the continuous current mode (CCM). Therefore, the equivalent single-switch model can be obtained by the averaged state-space method.

In state 1 and state 2, the voltage v_L expressed as the sum of two inductor voltages v_{LA} and v_{LB} can be obtained by Kirchhoff's voltage law (KVL), respectively.

$$\text{State 1}: \begin{matrix} v_s > 0 \\ s(t) = High \end{matrix} \quad \begin{cases} v_L = v_{LA} = v_s + v_{C2} - V_{ON} - i_L r_L \\ v_{LB} = 0 \end{cases} \tag{2}$$

$$\text{State 2}: \begin{matrix} v_s > 0 \\ s(t) = Low \end{matrix} \quad \begin{cases} v_L = v_{LA} = v_s - v_{C1} - V_{ON} - i_L r_L \\ v_{LB} = 0 \end{cases} \tag{3}$$

Similarly, the voltage v_L can be expressed as in (4) and (5) when $v_s < 0$, respectively.

$$\text{State 3}: \begin{matrix} v_s < 0 \\ s(t) = High \end{matrix} \quad \begin{cases} v_{LA} = 0 \\ v_L = v_{LB} = v_s - v_{C1} + V_{ON} - i_L r_L \end{cases} \tag{4}$$

$$\text{State 4}: \begin{matrix} v_s < 0 \\ s(t) = Low \end{matrix} \quad \begin{cases} v_{LA} = 0 \\ v_L = v_{LB} = v_s + v_{C2} + V_{ON} - i_L r_L \end{cases} \tag{5}$$

In order to combine the voltage equation in (2)-(5), an operator $sign(v_s)$ is introduced and it is defined as

$$sign(v_s) = \begin{cases} +1, & v_s \ge 0 \\ -1, & v_s < 0 \end{cases} \tag{6}$$

By combining (2) and (4), the voltage v_L during $s(t) = High$ can be expressed as

$$v_L = v_s - sign(v_s)V_{ON} - \frac{1}{2}(v_{C1} - v_{C2}) + \frac{sign(v_s)}{2}V_o - i_L r_L \tag{7}$$

where the voltage V_o is the sum of the two capacitor voltages $V_o = v_{C1} + v_{C2}$ and the inductor current is the sum of the two inductor currents $i_L = i_{LA} + i_{LB}$.

Similarly, the inductor voltage v_L in (3) and (5) during $s(t) = Low$ can be expressed as

$$v_L = v_s - sign(v_s)V_{ON} - \frac{1}{2}(v_{C1} - v_{C2}) - \frac{sign(v_s)}{2}V_o - i_L r_L \tag{8}$$

From (7) and (8), the equivalent single-switch model for DBHB PFC converter can be generated as plotted in Fig. 4.

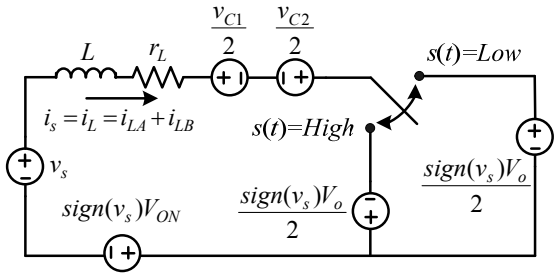

Fig. 4. Equivalent single-switch model.

In Fig. 2, the switching signal $s(t)$ is generated from the comparison between the control signal v_{cont} and the triangular signal v_{tri} varying between 0 and $\hat{V}_{tri}$. Therefore, the turn-on time of $s(t) = High$ is calculated by $(v_{cont}/\hat{V}_{tri}) \cdot T_s$, and the turn-off time during $s(t) = Low$ is $[1 - (v_{cont}/\hat{V}_{tri})] \cdot T_s$.

Eventually, by applying the time-averaging approach, the average inductor voltage $\langle v_L \rangle_{T_s}$ can be obtained from multiplying (7) and (8) by turn-on time and turn-off time, respectively.

$$\langle v_L \rangle_{T_s} = \begin{pmatrix} \langle v_s \rangle_{T_s} - sign(v_s)V_{ON} - \frac{1}{2}\left(\langle v_{C1} \rangle_{T_s} - \langle v_{C2} \rangle_{T_s}\right) \\ -\frac{sign(v_s)V_o}{2}\left(1 - 2\frac{v_{cont}}{\hat{V}_{tri}}\right) - \langle i_L \rangle_{T_s} r_L \end{pmatrix} \tag{9}$$

C. Balanced Capacitor Voltages

From Fig. 2, the input current i_s can be expressed as

$$i_s = i_{C1} - i_{C2} = C\frac{dv_{C1}}{dt} - C\frac{dv_{C2}}{dt} \tag{10}$$

For the desired PFC function, the input current i_s should be sinusoidal in phase with the input voltage $v_s = \hat{V}_s \sin(\omega t)$, and it can be expressed as $i_s = \hat{I}_s \sin(\omega t)$. Therefore, from (10), the steady-state difference between two capacitor voltages can be expressed as

$$v_{C1} - v_{C2} = \frac{1}{C}\int i_s dt = \frac{1}{C}\int \hat{I}_s \sin(\omega t) dt = -\frac{\hat{I}_s}{\omega C}\cos(\omega t) \tag{11}$$

With neglecting the power loss, the instantaneous input power $v_s i_s$ would be equal to the DC-side instantaneous power.

$$v_s i_s = \frac{1}{2}\hat{V}_s \hat{I}_s (1 - \cos 2\omega t) \approx V_o\left(\frac{V_o}{R_L} + \frac{i_{C1} + i_{C2}}{2}\right) \tag{12}$$

where the DC-side instantaneous power is expressed as the product of the constant voltage V_o and the sum of current flowing through the load resistor and the capacitors. By

canceling the constant terms $0.5\hat{V}_s\hat{I}_s$ and V_o^2/R_L in (12), the sum of the capacitor currents can be roughly obtained by

$$i_{C1}+i_{C2}\approx-\frac{\hat{V}_s\hat{I}_s}{V_o}\cos(2\omega t) \tag{13}$$

It follows that the output voltage $v_{C1}+v_{C2}$ with consideration of the double-line-frequency ripple can be expressed as

$$v_{C1}+v_{C2}\approx V_o-\frac{1}{C}\int\frac{\hat{V}_s\hat{I}_s\cos(2\omega t)}{V_o}dt=V_o-\frac{\hat{V}_s\hat{I}_s\sin(2\omega t)}{2\omega CV_o} \tag{14}$$

By solving (11) and (14), the steady-state capacitor voltages v_{C1} and v_{C2} can be obtained by

$$v_{C1}\approx\frac{V_o}{2}-\frac{\hat{I}_s}{2\omega C}\cos(\omega t)-\left(\frac{\hat{V}_s}{2V_o}\right)\frac{\hat{I}_s}{2\omega C}\sin(2\omega t) \tag{15}$$

$$v_{C2}\approx\frac{V_o}{2}+\frac{\hat{I}_s}{2\omega C}\cos(\omega t)-\left(\frac{\hat{V}_s}{2V_o}\right)\frac{\hat{I}_s}{2\omega C}\sin(2\omega t) \tag{16}$$

Obviously, both capacitor voltages have the same terms, and the only difference is the sign of the line-frequency components $\cos(\omega t)$. In addition, the line-frequency components $\cos(\omega t)$ of capacitor voltages in (15) and (16) are larger than their double-line frequency components $\sin(2\omega t)$ because that the coefficient $\hat{V}_s/(2V_o)$ is smaller than 0.25. Thus, the line-frequency component $\cos(\omega t)$ is the dominant component in each capacitor voltage. It is noted that only the double-line-frequency component $\sin(2\omega t)$ can be found in the output voltage V_o because that the line-frequency components in (15)-(16) are cancelled out by each other in the steady-state balanced condition.

Due to the half-bridge topology, both capacitor voltages v_{C1} and v_{C2} should be balanced and be kept larger than the amplitude $\hat{V}_s$ of the input voltage v_s. Therefore, with consideration of the dc component and the line-frequency component in (15) and (16), the design of capacitance *C* can be roughly obtained by

$$C>\frac{\hat{I}_s}{\omega(V_o-2\hat{V}_s)} \tag{17}$$

D. Output Voltage Ripple for Imbalanced Loads

For balanced loads, the line-frequency component in capacitor voltages would be cancelled out by each other. Thus, the double-line-frequency ripple in output voltage is dominant.

But, for imbalanced loads, the line-frequency component in capacitor voltages will not be cancelled out, and the significant line-frequency component would show in the output voltage ripple $V_{o,ripple}$.

$$V_{o,ripple}\approx a\cos(\omega t) \tag{18}$$

where the coefficient *a* may be either positive or negative.

When an extra resistor is connected to the capacitor C_1, the observed voltage ripple is near $V_{o,ripple}\approx a\cos(\omega t)$, $a<0$. On the other hand, when an extra resistor is connected to the capacitor C_2, the observed voltage ripple is near $V_{o,ripple}\approx a\cos(\omega t)$, $a>0$.

III. Proposed Current Sensorless Control

A. Current Sensorless Control

In order to reduce the current sensor, the single-loop current sensorless control is proposed. The proposed current sensorless control is able to regulate the output voltage V_o and shape the input current i_s in phase with the input voltage v_s.

For the PFC function, the desired average current can be expressed as the $\sin(\omega t)$ function

$$\langle i_s\rangle_{T_s}=\langle i_L\rangle_{T_s}=\hat{I}_s\sin(\omega t) \tag{19}$$

Therefore, the average inductor voltage $\langle v_L\rangle_{T_s}$ should be forced to the $\cos(\omega t)$ expression

$$\langle v_L\rangle_{T_s}=L\frac{d\langle i_L\rangle_{T_s}}{dt}=\omega L\hat{I}_s\cos(\omega t)=\hat{V}_L\cos(\omega t) \tag{20}$$

where the value $\hat{V}_L=\omega L\hat{I}_s$ can be seen as the amplitude of the inductor voltage $\langle v_L\rangle_{T_s}$. By substituting (19) and (20) into (9), the control signal v_{cont} can be obtained as

$$v_{cont}=\frac{\hat{V}_{tri}}{2}-\frac{\hat{V}_{tri}}{V_o^*}\left\{|v_s|-\left[\begin{array}{l}V_{ON}+\frac{1}{2}sign(v_s)(v_{C1}-v_{C2})\\+\hat{V}_L\left(h_1+h_2\frac{r_L}{\omega L}\right)\end{array}\right]\right\} \tag{21}$$

where $|\cdot|$ is the absolute (ABS) operator and the terms $h_1=\cos(\omega t)sign(v_s)$ and $h_2=|\sin(\omega t)|$ are synchronously generated from the input voltage v_s.

The proposed current sensorless control scheme in (21) is plotted in Fig. 5. A simple integrator controller is used to regulate the output voltage and tune the voltage signal $\hat{V}_L$.

$$\hat{V}_L=\frac{K_i}{s}v_{error}=\frac{K_i}{s}(V_o^*-v_{C1}-v_{C2}) \tag{22}$$

From (12) and (20), the average power *P* can be expressed as

$$P=\frac{\hat{V}_s\hat{I}_s}{2}=\frac{\hat{V}_s}{2}\left(\frac{\hat{V}_L}{\omega L}\right) \tag{23}$$

It shows that the average power is proportional to the controller output $\hat{V}_L$. From Fig. 5, the integrator tunes the voltage amplitude signal $\hat{V}_L$. It follows that a simple integrator controller is able to balance the average power flow and thus, regulate the output voltage.

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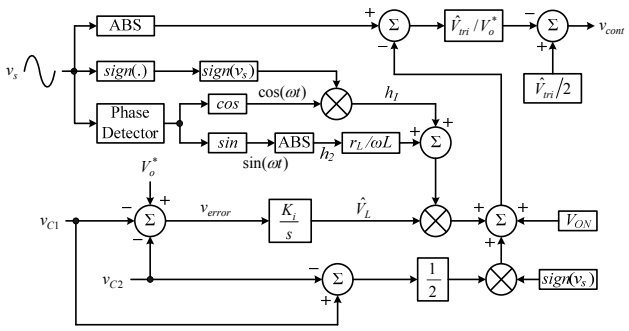

Fig. 5. Proposed current sensorless control scheme.

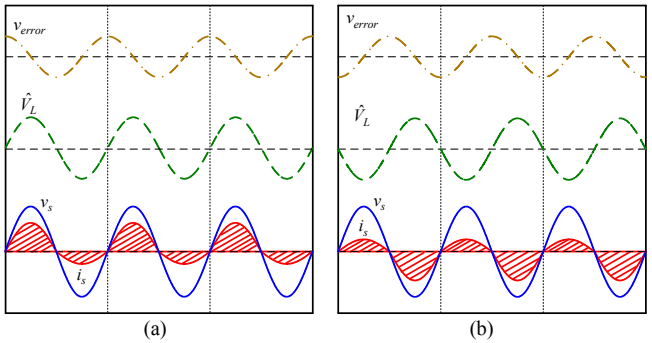

Fig. 6. Illustration of natural capacitor voltage balancing: (a) transient response after an extra resistor is connected to C_1; (b) transient response after an extra resistor is connected to C_2.

B. Natural Capacitor Voltage Balancing

From Fig. 5, the amplitude of voltage signal $\hat{V}_L$ is determined from the difference between the output voltage V_o and the voltage command V_o^* through an integrator controller. From (18), the voltage error v_{error} in the imbalanced condition can be approximated as

$$v_{error} \approx V_{error} - a\cos(\omega t) \tag{24}$$

where V_{error} is the dc voltage error and the line-frequency component is dominant ripple.

After the integrator controller with gain K_i, the controller output $\hat{V}_L$ from (22) can be obtained as

$$\hat{V}_L = \hat{V}_{L0} - K_i \frac{a}{\omega}\sin(\omega t) \tag{25}$$

where $\hat{V}_{L0}$ is the dc value of $\hat{V}_L$.

When an extra resistor is connected to the capacitor C_1, the capacitor voltages turn to be imbalanced. The feedback voltage error v_{error} is near to $a\cos(\omega t)$ with $a<0$. Then, the ripple $-(a/\omega)\sin(\omega t)$ observed in the controller output $\hat{V}_L$ would be in phase with the input voltage $\hat{V}_s\sin(\omega t)$. Thus, the yielded current in positive half-cycle would be larger than that in negative half-cycle as shown in Fig. 6(a), which contributes to more charges stored in the capacitor C_1 than C_2, and the balance between two capacitor voltages.

On the other hand, when an extra resistor is connected to the capacitor C_2, the observed ripple in the controller output $\hat{V}_L$ would be near $-(a/\omega)\sin(\omega t)$ where $a>0$. Thus, the yielded current in negative half-cycle is larger than that in positive half-cycle as shown in Fig. 6(b), which brings more charges to capacitor C_2 than C_1, and balances the capacitor voltages.

Consequently, the proposed current sensorless control is able to balance the capacitor voltages without introducing the additional voltage balancing loop.

C. Small-Signal Transfer Functions

The small-signal transfer function between the output voltage ΔV_o and the controller output $\Delta\hat{V}_L$ can be obtained from the power balance between the input power P_s, the load power P_R and two capacitor powers P_{C1}, P_{C2}. The input power P_s with small perturbation ΔP_s can be expressed as

$$P_s + \Delta P_s = \frac{\hat{V}_s\left(\hat{V}_L + \Delta\hat{V}_L\right)}{2\omega L} = \frac{\hat{V}_s\hat{V}_L}{2\omega L} + \frac{\hat{V}_s\Delta\hat{V}_L}{2\omega L} \tag{26}$$

The load power P_R with small perturbation ΔP_R can be represented by the voltage command V_o^* plus the output voltage perturbation ΔV_o.

$$P_R + \Delta P_R = \frac{\left(V_o^* + \Delta V_o\right)^2}{R_L} \approx \frac{\left(V_0^*\right)^2}{R_L} + \frac{2V_o^*\Delta V_o}{R_L} \tag{27}$$

The two capacitor power perturbations ΔP_{C1} and ΔP_{C2} can be depicted by the output voltage perturbation ΔV_o, respectively.

$$\Delta P_{C1} = \frac{d}{dt}\left[\frac{1}{2}C\left(\frac{1}{2}V_o^* + \frac{1}{2}\Delta V_o\right)^2\right] \approx \frac{1}{4}CV_o^*\frac{d\Delta V_o}{dt} \tag{28}$$

$$\Delta P_{C2} = \frac{d}{dt}\left[\frac{1}{2}C\left(\frac{1}{2}V_o^* + \frac{1}{2}\Delta V_o\right)^2\right] \approx \frac{1}{4}CV_o^*\frac{d\Delta V_o}{dt} \tag{29}$$

Therefore, the balance between the power perturbations $\Delta P_s = \Delta P_R + \Delta P_{C1} + \Delta P_{C2}$ can yield the following small-signal transfer function $G_s(s)$.

$$G_s(s) = \frac{\Delta V_o}{\Delta\hat{V}_L} = \frac{\hat{V}_s}{2\omega L}\frac{2}{CV_o^*\left(s + \frac{4}{CR_L}\right)} \tag{30}$$

By using an integrator controller $G_c(s) = K_i/s$, the second-order closed-loop transfer function of the output voltage ΔV_o and the voltage command ΔV_o^* can be found in (31).

$$\frac{\Delta V_o}{\Delta V_o^*}=\frac{K_i\dfrac{\hat{V}_s}{\omega LCV_o^*}}{s^2+\dfrac{4}{CR_L}s+K_i\dfrac{\hat{V}_s}{\omega LCV_o^*}} \tag{31}$$

The block diagram of closed-loop voltage control is plotted in Fig 7. The bandwidth (BW) of the voltage control loop (31) can be obtained by the following formula

$$BW=\omega_n\left[\left(1-2\xi^2\right)+\sqrt{4\xi^4-4\xi^2+2}\right]^{\frac{1}{2}} \tag{32}$$

where $\omega_n=\sqrt{\dfrac{K_i\hat{V}_s}{\omega LCV_o^*}}$ and $\xi=\dfrac{2}{\omega_n CR_L}$.

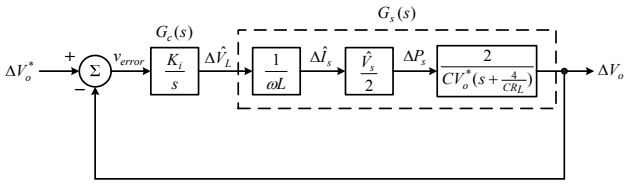

Fig. 7. Block diagram of closed-loop voltage control.

IV. Simulation Results

In this section, some simulation results of the proposed current sensorless control for dual-boost half-bridge PFC converter are provided. The simulation parameters and some nominal values are listed in Table II. The root-mean-square (rms) value of input voltage v_s is 110 V and the line frequency f is 60 Hz. The voltage controller is a simple integrator which is used to tune the controller output $\hat{V}_L$.

TABLE II
Simulation Parameters

Input voltage (rms)	$v_s=110\text{V}$
Output voltage command	$V_o^*=400\text{V}$
Switching frequency	$f_s=45\text{kHz}$
Line frequency	$f=60\text{Hz}$
Inductances	$L_A=L_B=2.23\text{mH}$
Inductor resistances	$r_{LA}=r_{LB}=0.4\Omega$
Capacitances	$C_1=C_2=1170\mu\text{F}$
Conduction voltage	$V_{ON}=2\text{V}$
Integrator gain	$K_i=30$

A. Steady-State Response

The steady-state waveforms with the output power 400W and 800W are plotted in Fig. 8(a) and Fig. 8(b), respectively. It is found that the input current i_s is sinusoidal in phase with the input voltage v_s. Moreover, the output voltage V_o is well regulated to the voltage command V_o^*=400V, and both output capacitor voltages v_{C1} and v_{C2} are well balanced at 200V.

Obviously, significant line-frequency components can be found in each capacitor voltage, but only double-line-frequency component can be found in the output voltage V_o, which meets the representation in (15)-(16).

In addition, the steady-state controller output $\hat{V}_L$ of output power 800W in Fig. 8(b) is near double the value of output power 400W in Fig. 8(a), which confirms equation in (23).

In summary, the proposed current sensorless control is able to achieve the steady-state PFC function without sensing the current and balance the capacitor voltages.

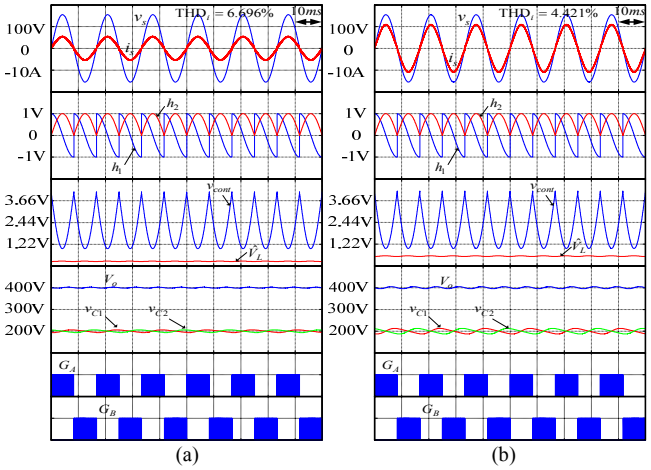

Fig. 8. Simulation results of steady-state waveforms: (a) 400W (R_L=400Ω); (b) 800W (R_L=200Ω).

With consideration of the parameter uncertainty, the simulated steady-state waveforms with 10% parameter deviation ($r_L=0.4\,\Omega\times1.1$, $L=2.23\,\text{mH}\times0.9$) at output power 400W and 800W are plotted in Fig. 9(a) and Fig. 9(b), respectively.

From Fig. 9, the result shows that the proposed current sensorless control is able to work well by the nominal control parameters. However, the parameter uncertainty would yield larger current harmonics than the nominal case in Fig. 8.

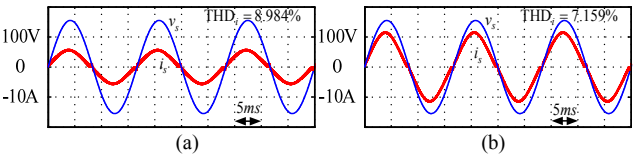

Fig. 9. Simulated steady-state waveforms with circuit parameters $r_L=0.4\,\Omega\times1.1$ and $L=2.23\,\text{mH}\times0.9$: (a) 400W (R_L=400Ω); (b) 800W (R_L=200Ω)

B. Transient Response

In order to evaluate the transient responses of the proposed current sensorless control, the load resistor is changed between 400Ω and 200Ω. Some simulation results are plotted in Fig. 10. The yielded input current i_s is still sinusoidal in phase with the input voltage v_s, and the output voltage V_o is stably regulated back to 400V during the change of the load resistor.

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The magnitude of input current i_s varies between 3.7A and 7.4A to provide sufficient average power to regulate the output voltage. The transient time of the voltage regulation are 54ms and 46ms, respectively. Thus, the simple integrator controller included in the voltage loop is able to regulate the output voltage.

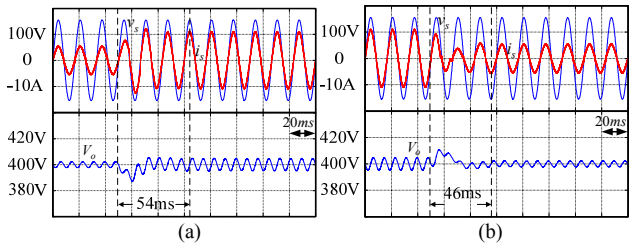

Fig. 10. Simulation results when the load resistor changes: (a) from 400W (R_L=400Ω) to 800W (R_L=200Ω); (b) from 800W (R_L=200Ω) to 400W (R_L=400Ω).

C. Natural Capacitor Voltage Balancing

To demonstrate the performance of the natural voltage balancing, some results are provided in this section.

At the steady-state condition 400W, an additional 100Ω resistor is suddenly connected to the capacitor C_1. The simulation results are plotted in Fig. 11(a), and its zoomed waveforms is plotted in Fig. 11(b). It can be found that the capacitor voltage v_{C1} gradually drops down to 155V, and the other capacitor voltage v_{C2} rises up to near 245V simultaneously due to the proposed current sensorless control.

From the zoomed waveforms in Fig. 11(b), significant line-frequency ripple can be found in the controller output $\hat{V}_L$ during the imbalanced condition. Fortunately, the ripple-rich voltage amplitude $\hat{V}_L$ contributes to the larger current in positive half-cycle than that in negative half-cycle. Then, the capacitor voltages are naturally balanced after the connected resistor is removed.

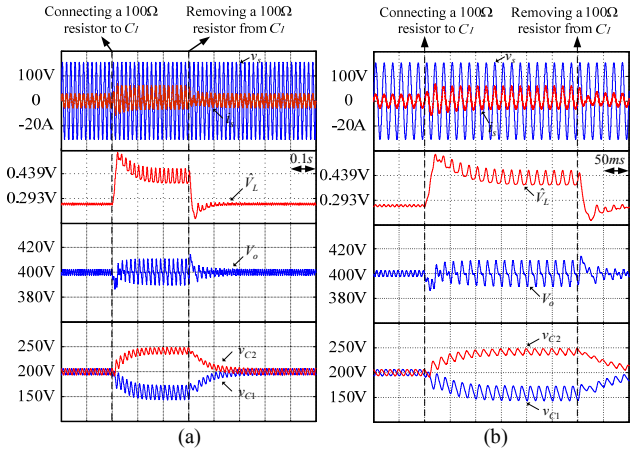

Fig. 11. Simulation results when a 100Ω resistor is connected to the capacitor C_1 and then removed: (a) original waveforms; (b) zoomed waveforms.

In Fig. 12(a), the extra 100Ω resistor is suddenly connected to the capacitor C_2. The capacitor voltages v_{C1} and v_{C2} gradually fluctuate to 245V and 155V, respectively, but the output voltage V_o is regulated to 400V. In addition, the controller output $\hat{V}_L$ during negative half-cycle is larger than that during positive half-cycle as shown in Fig. 12(b). After the resistor is connected across the capacitor C_2, the magnitude of the yielded current i_s during the negative half-cycle is larger than that during positive half-cycle until both capacitor voltages are balanced.

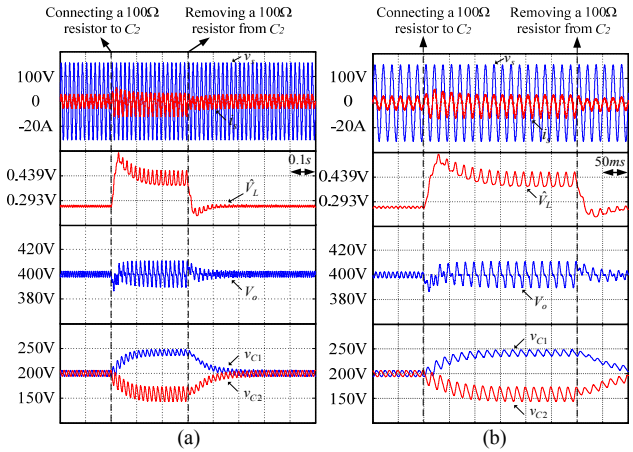

Fig. 12. Simulation results when a 100Ω resistor is connected to the capacitor C_2 and then removed: (a) original waveforms; (b) zoomed waveforms.

From the simulation results, the characteristics of natural capacitor voltage balancing with the proposed control method are validated.

V. Experimental Results

To evaluate the proposed current sensorless control, an 800W prototype converter is implemented in Fig. 13. The proposed control method is implemented in a DSP-based system by using TI TMS320F28335 as shown in Fig. 13. The experimental parameters are the same as those in Table II. Additionally, the block diagram of experiment setup is plotted in Fig. 14 for reference. Because there is no D/A function in the TI DSP chip, four external D/A circuits are designed to plot the control variables in the oscilloscope.

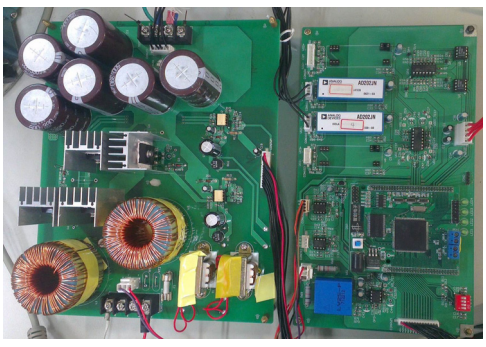

Fig. 13. Implemented dual-boost half-bridge PFC converter with DSP chip.

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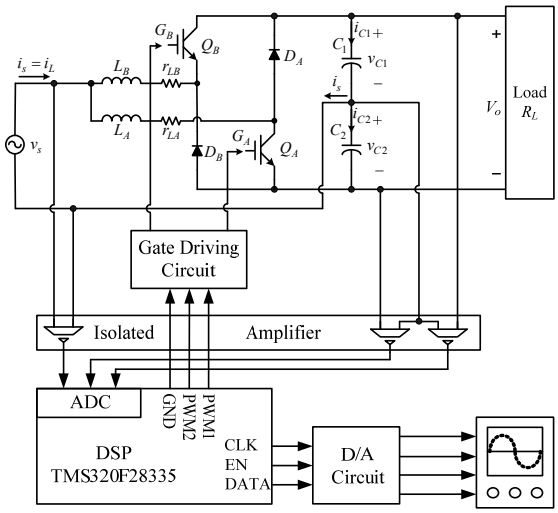

Fig. 14. Block diagram of experiment setup.

A. Steady-State Response

The experimental steady-state waveforms of 400W and 800W are plotted in Fig. 15(a) and Fig. 15(b), respectively. Individual inductor currents i_{LA} and i_{LB} are also plotted for comparison. The inductor currents i_{LA} and i_{LB} flows during the positive and negative half-cycle, respectively.

The output voltage V_o is well regulated to 400V, and the yielded input current i_s is always sinusoidal in phase with the distorted voltage v_s. Both capacitor voltages v_{C1} and v_{C2} are balanced at 200V, and their significant line-frequency ripples can be found especially in high power level of Fig. 15(b). Only double-line-frequency ripple can be found in the output voltage V_o in steady-state balanced condition.

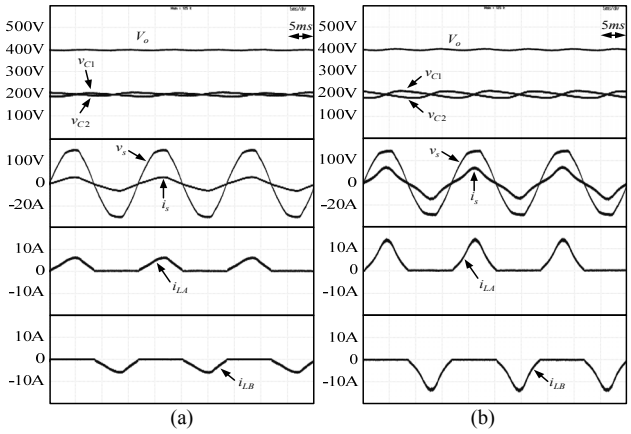

Fig. 15. Experimental results of steady-state waveform: (a) 400W (R_L=400Ω); (b) 800W (R_L=200Ω).

Table III shows the detailed harmonic currents of Fig. 15 with IEC-61000-3-2 standard for comparison. Furthermore, the harmonic current limitations for class A are independent of the power level, and the limitations for class D are required the power level which is 75W up to and not exceeding 600W.

It is noted that experimental harmonic currents always comply with the IEC-61000-3-2 standard. The measured total harmonic distortion of current (THD_i) are 9.545% and 14.019% at 400W and 800W, respectively, and the recorded power factors (PF) are near unity.

TABLE III
HARMONICS OF EXPERIMENTAL RESULTS

Output Power		400 W (R_L=400 Ω)		800 W (R_L=200 Ω)	
Harmonics	Class A	Class D	Fig. 15(a)	Class D	Fig. 15(b)
Fundamental	X	X	3.731A		7.705A
3rd	2.30A	1.36A	0.339A		1.032A
5th	1.14A	0.76A	0.042A		0.238A
7th	0.77A	0.40A	0.084A		0.165A
9th	0.40A	0.20A	0.015A		0.051A
11th	0.33A	0.14A	0.019A		0.051A
13th	0.21A	0.1184A	0.028A		0.071A
15th	0.15A	0.1027A	0.011A		0.038A
17th	0.1324A	0.0906A	0.009A		0.033A
19th	0.1184A	0.0811A	0.014A		0.040A
PF			0.9939		0.9841
THD_i (%)			9.545 %		14.019 %

From the provided experimental results, the proposed current sensorless control is able to achieve PFC function even when the input voltage is distorted. Furthermore, the measured efficiency for various load resistance are tabulated in Table IV, where R_L is load resistance, P_s is the input power and P_R is load power. The converter's overall efficiency is greater than 93.63%. This performance is acceptable for the current sensorless control.

TABLE IV
MEASURED EFFICIENCY FOR VARIOUS LOAD RESISTANCES

R_L (Ω)	P_s (W)	P_R (W)	Efficiency (%)
200	808.6	757.1	93.63
300	558.9	527.9	94.45
400	416.9	395.6	94.77
500	313.7	301.1	95.98

B. Transient Response

In order to validate the transient performances of the proposed current sensorless control, the load resistor is changed between 400Ω (400W) and 200Ω (800W) and the results are plotted in Fig. 16(a) and Fig. 16(b), respectively.

From the experimental waveforms, both input currents i_s are always sinusoidal in phase with the input voltage v_s during the transient condition. In order to regulate the output voltage V_o, the integrator controller tunes the controller output $\hat{V}_L$ between 0.244 and 0.582 to provide the sufficient average power.

With the change of load resistor, both capacitor voltages have the same changing direction. Thus, neither line-frequency ripple nor double-line frequency ripple can be found in the output voltage V_o and the controller output $\hat{V}_L$ during the change of the load resistor.

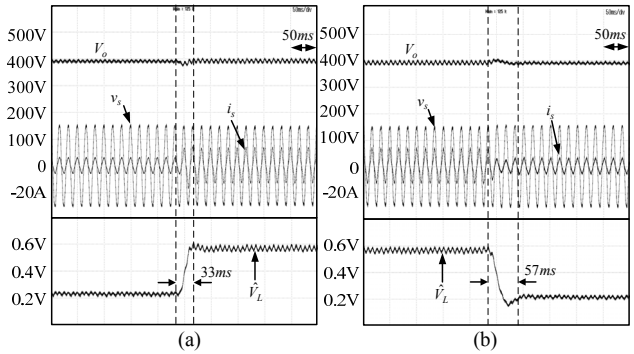

Fig. 16. Experimental results when the load resistor changes: (a) from 400W (R_L=400Ω) to 800W (R_L=200Ω); (b) from 800W (R_L=200Ω) to 400W (R_L=400Ω).

C. Natural Capacitor Voltage Balancing

To evaluate the natural voltage balancing performance, an extra 100Ω resistor is suddenly connected across the capacitor C_1 and C_2, respectively, and then removed. The measured waveforms are plotted in Fig. 17 and Fig. 18, respectively. Unlike the change of load resistor, the capacitor voltages have different changing direction, and thus the significant line-frequency ripple can be found in the output voltage V_o and the controller output $\hat{V}_L$ until the connected resistor is removed.

When an additional resistor 100Ω is suddenly connected across capacitor C_1 and then removed, the measured waveforms are plotted in Fig. 17(a). The capacitor voltage v_{C1} drops to 156V and the voltage v_{C2} rises to 244V within 0.3 seconds. From the zoomed waveforms in Fig. 17(b), the controller output $\hat{V}_L$ in positive half-cycle is higher than that in negative half-cycle due to its ripple.

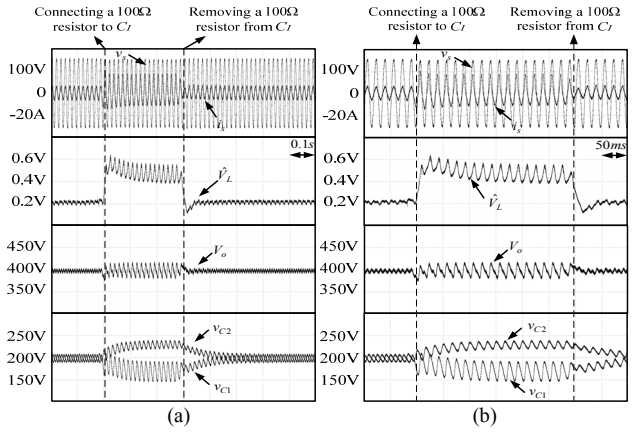

Fig. 17. Experimental results when a 100Ω resistor is connected to the capacitor C_1 and then removed: (a) original waveforms; (b) zoomed waveforms.

The resulting current magnitude of input current i_s during positive half-cycle is higher than that during negative half-cycle, which brings more charges to the capacitor C_1 than the capacitor C_2. Thus, the proposed current sensorless control is able to balance the capacitor voltage after the resistor is connected across capacitor C_1.

With consideration of the other condition, an extra 100Ω resistor is suddenly connected across the capacitor C_2 and then removed. In Fig. 18(a), the capacitor voltage v_{C1} rises to 243V and v_{C2} drops to 157V. From the zoomed waveforms in Fig. 18(b), the significant line-frequency ripple can be found in the output voltage V_o and the controller output $\hat{V}_L$.

Fortunately, the controller output $\hat{V}_L$ is higher during the negative half-cycle than that during the positive half-cycle. It follows that the magnitude of input current i_s during negative half-cycle is higher than that during the positive half-cycle. The larger current amplitude contributes to more charges stored to the capacitor C_2 than C_1. Eventually, both capacitor voltages v_{C1} and v_{C2} are balanced at 200V.

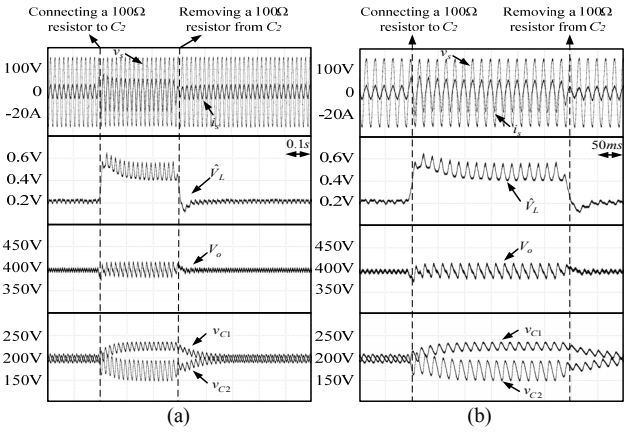

Fig. 18. Experimental results when a 100Ω resistor is connected to the capacitor C_2 and then removed: (a) original waveforms; (b) zoomed waveforms.

From the experimental results, the proposed current sensorless control method is able to meet the PFC function not only in the steady-state condition, but also in the transient condition. At the same time, the voltage ripples in the output voltage V_o and the controller output $\hat{V}_L$ benefit the voltage balance. Thus, the proposed control method is also to naturally balance the capacitor voltages without introducing any voltage balancing loop.

VI. CONCLUSION

The single-switch model for DBHB PFC converter has been developed. The current sensorless control method for DBHB PFC converter has been proposed and implemented in this paper. The integrator-type voltage controller is able to regulate the output voltage and balance the capacitor voltages. The proposed control strategy effectively achieves PFC function in steady-state condition and transient condition. Moreover, the capacitor voltages can be naturally balanced by the proposed control method. From the simulation and experimental results of 800W prototype converter, the proposed current sensorless control method is demonstrated. This control method can be

used to the half-bridge PFC converter due to the same single-switch model.

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